HPES
High Performance Embedded Systems

EEE4120F

University of Cape Town • iYunivesithi yaseKapa • Universiteit van Kaapstad

SPES BONA

High Performance Embedded Systems

Lecture 13

YODA Project & Discussion of Digital Accelerators

Presented by

Simon Winberg

Lecture Overview

- YODA Project
- Digital accelerators
- Project Milestones
- YODA 'Conference'

A SCENARIO…

Reconfigurable Computing

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The Reconfigurable Hardware Platform

More colloquially, at the start
of the mission: “The Doorstop”

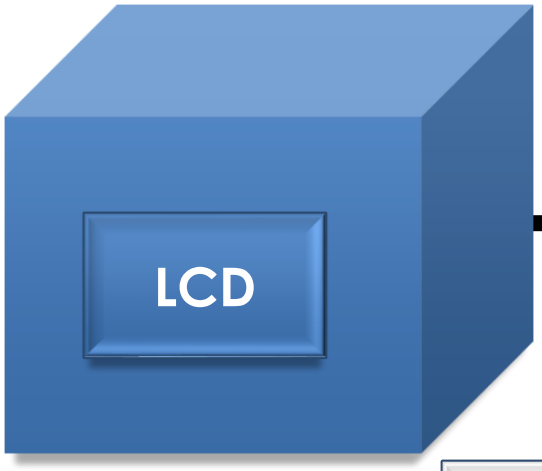
The Reconfigurable Hardware Platform

More colloquially, at the start of the mission: "The Doorstop"

Like most doorstops, this one starts out being a lump that is in the way; although it may have all sorts of potential if you…

… apply your mind, you must!

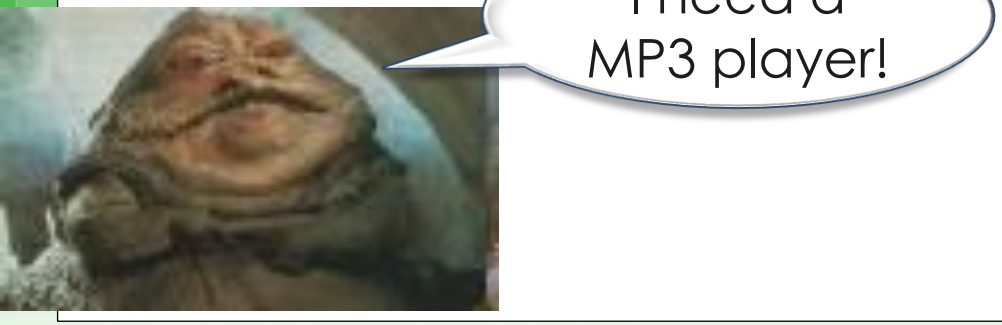
Scenario: Reconfigurable platform



reconfigure

Doorstop

Jabba the Hutt says:



(you may need some additional external items in order to make use of the reconfigured system)

reconfigure

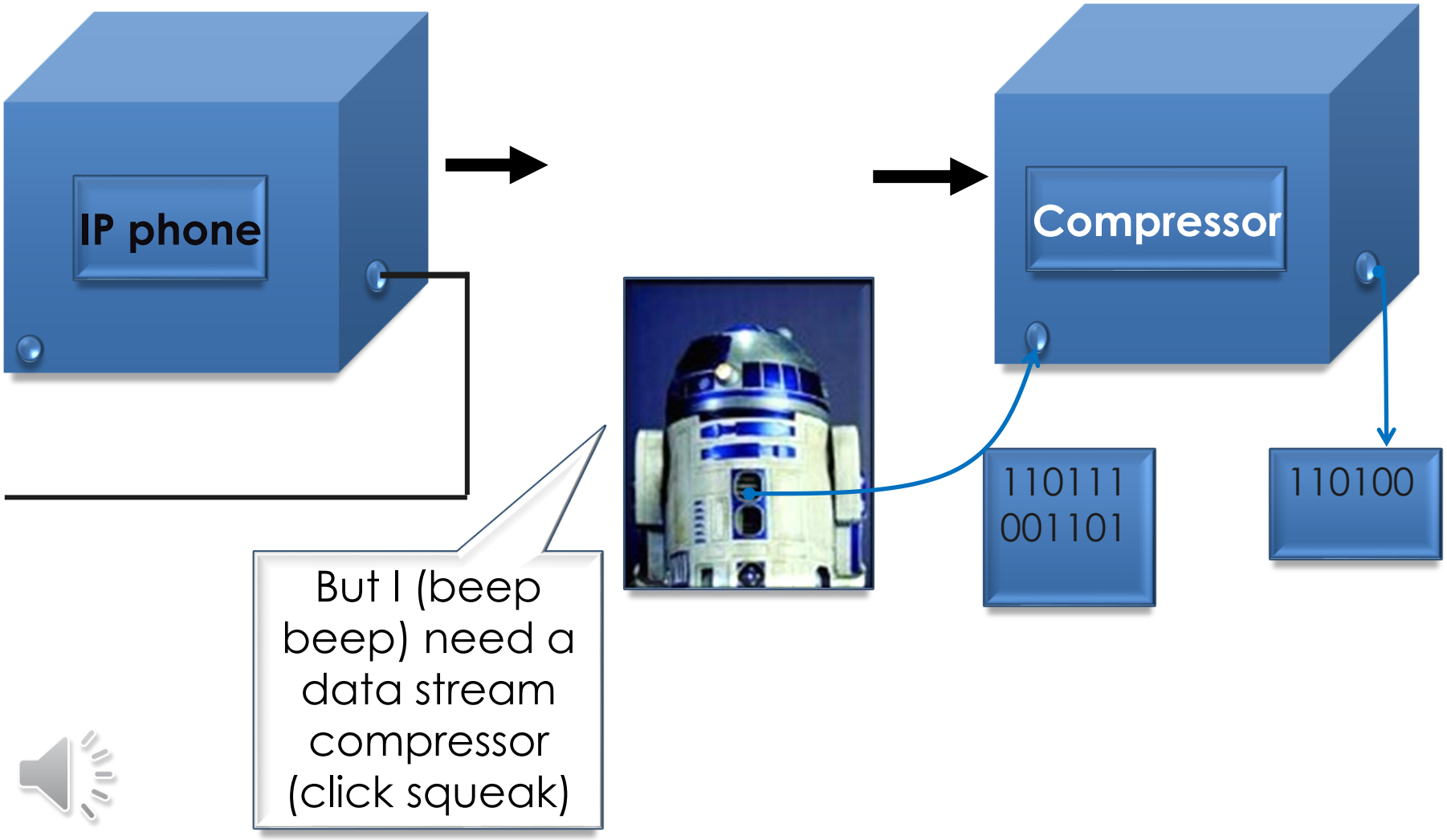
The Hutt is satisfied.
But now wants more…

Yak yak *

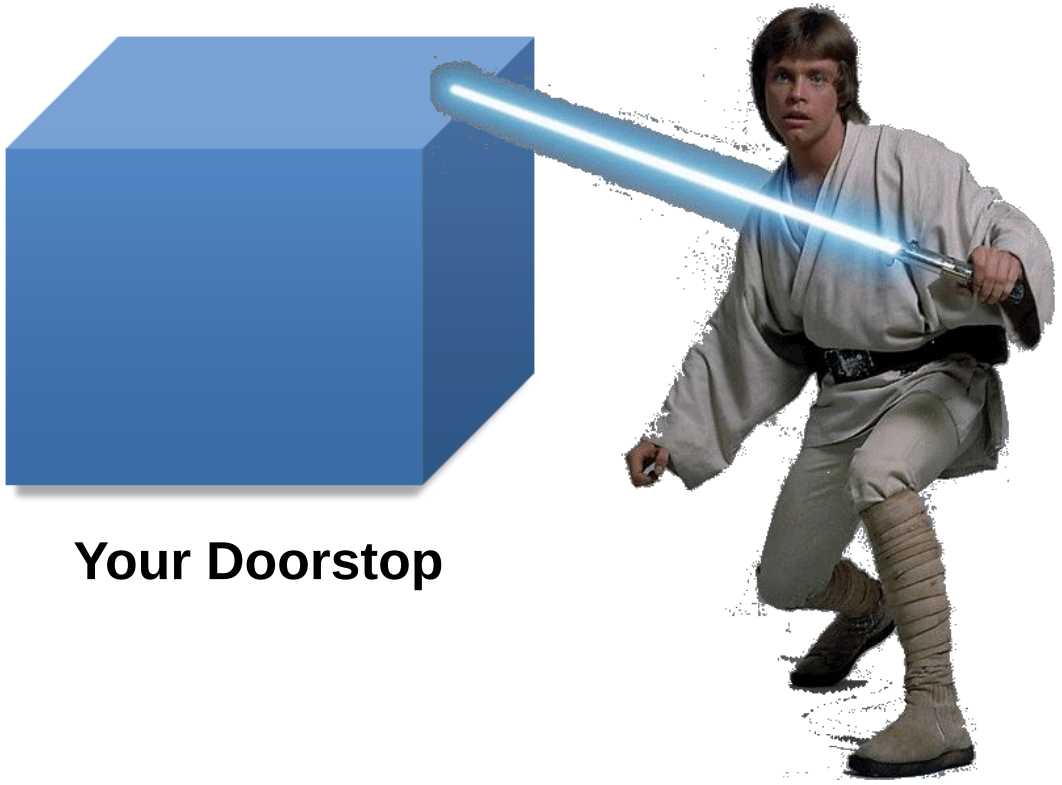
Now I need an IP phone!

In case you're wondering what sort of client Jabber is like, especially if he had an MP3 player, you could watch this amusing skit: https://www.youtube.com/watch?v=H2ftVPk-WZw

With the expanding product line your RC development firm is likely to get more and more (and even more unlikely) clients… such as



But what is this "doorstop" of which you speak?



Your Doorstop

A "doorstop" for your enlightenment and education…

But first: patience you must have as this knowledge will be revealed once you are ready…

Getting ready for your "doorstop"…

Choice of either …

A real doorstop …

Using FPGA Evaluation Kit:
e.g. Nexys 4 or Nexys A7

OR

A virtual doorstop

Simulation-based system
e.g. iVerilog or Vivado Simulator

Reconfigurable Computing EEE4120F

A brief overview of Reconfigurable Computing operation…

Option A: FPGA-based Digital Accelerator

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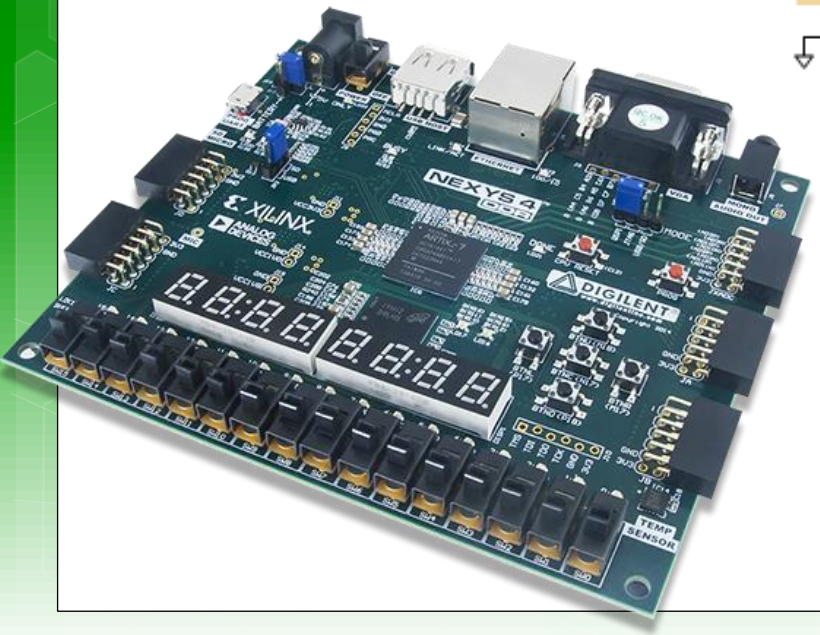
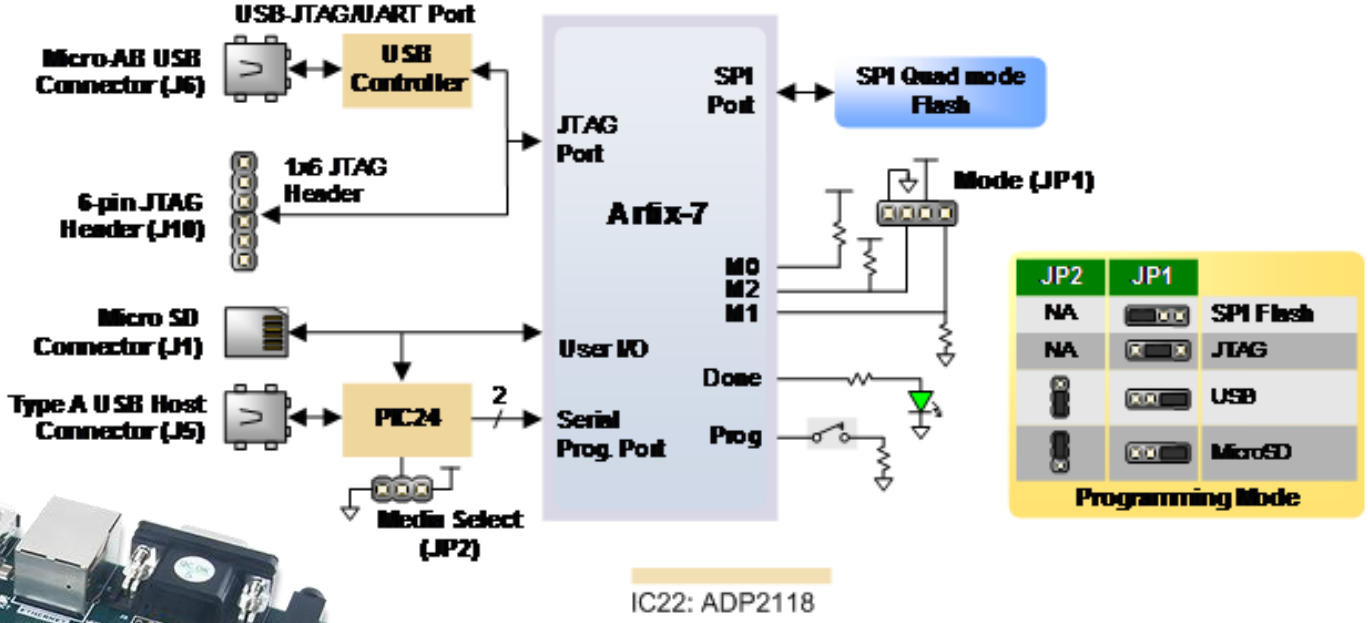
Nexys4 DDR: The evaluation board to be used in the laboratories…

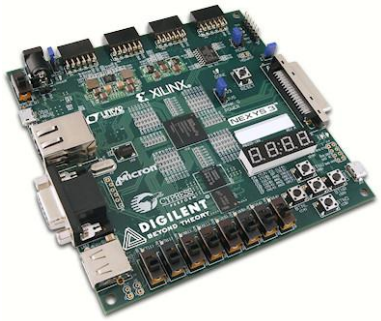
The other Nexys versions are quite similar



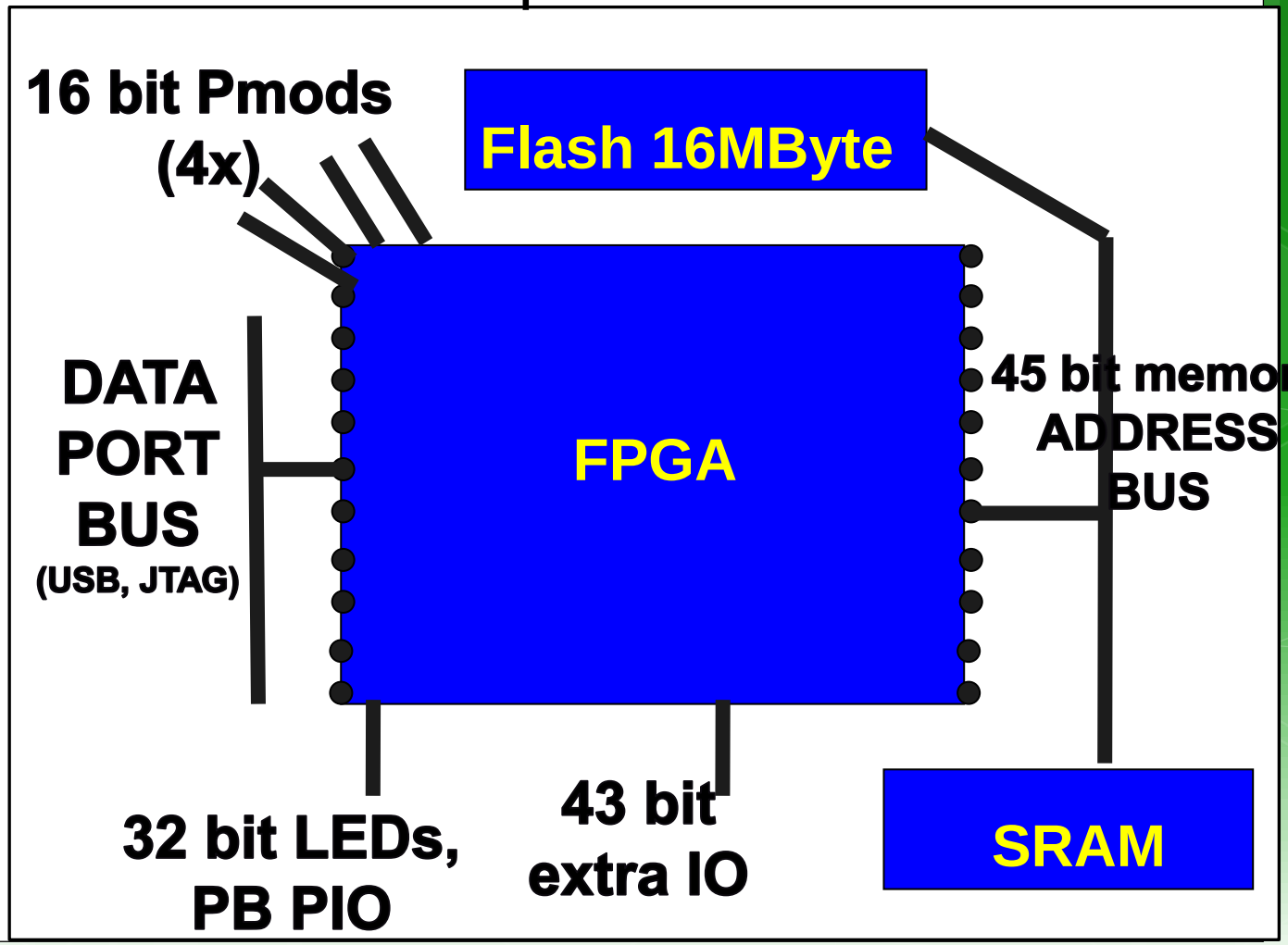


Source: https://digilent.com/reference/programmable-logic/nexys-4/reference-manual

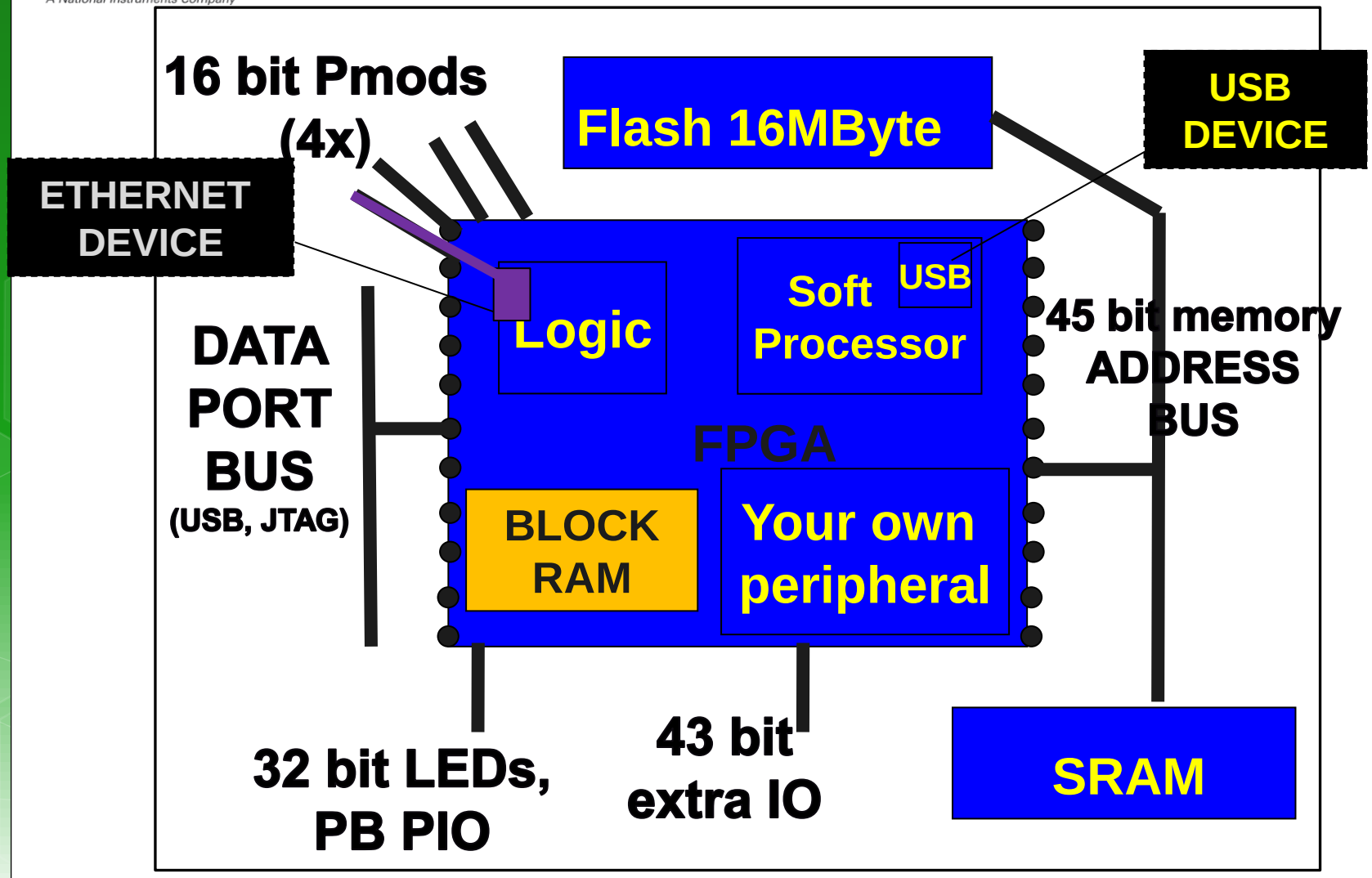
Nexys:
The evaluation board to be used in the laboratories…



Simplified Model



Nexys:
Simplified Model



Want your own Nexys?

If you want your own Nexys you can order one from the DigilentInc website. The Nexys A7 is somewhat pricier than the Nexys4 and 3 (of which stock may be limited, if not discontinued). Nexys4 about $179 with education discount. The lower cost (and simpler) option is the Basys™3 Artix-7 FPGA Board, about $79; it has much of the peripherals as the Nexys4 has but cut down in other aspects. There is of course also ebay.com (still pricy, maybe save 50%).

There are enough to go round for labs if working as teams. If enough students would like their own Nexys board it's a good idea to group all into one order to save on the postage costs (the postage is about $50 or R500, only courier options are available).

If you decide to get your own Nexys, I recommend the NexysA7 or lower cost the CmodA7 (which I plan to use next year) if you can afford it since they're the bigger and more fancy FPGA options.

http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,1184&Prod=NEXYS4

http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,897&Prod=NEXYS3

http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,1288&Prod=BASYS3

Option B: Simulation-based Digital Accelerator

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Simulated Digital Accelerator

- The simulator can't access real IO. You would need to plan test vectors that you somehow load into the simulator.
- Similarly, if you have a front-end you may need to have a bit of a manual intervention in your demonstration, e.g.:
  - A simple GUI that outputs a test vector, that your testbench can then load and the simulator shows how signals change.
- A simulated approach is nevertheless a useful and authentic learning experience, as this approach is often applied in industry and in research projects to inspecting viability of a potential hardware / SoC design without going to the expense of fabricating it.
- For some applications, e.g. needing large input data, a simulation approach may offer much benefit and flexibility (as the evaluation boards we use do allow for very many input or output pins which may be required for systems working with long words and large data volumes).

Choosing an option: Arguing you case

- Ideally, you should provide motivation for why you decided to go for Option A of using a real FPGA or Option B using a simulator (not just because you want to hone your skills in the one or the other technology)
  - *Obvious crossover aspect:* generally, all projects will involve aspects of Option B… i.e. would need simulation. No coincidence for naming this one: Option B can be a backup or fallback position for an Option A project.

About YODA

YODA Project: Your Own Digital Accelerator

Reconfigurable Computing

Final Hand-in date: 15 May (last week of lectures)

What's A Digital Application Accelerator?

- An add-on card* or [reconfigurable] co-processor used to speed-up processing for a particular solution
- 'Digital' - comprises digital logic/circuitry to speed-up computation
- A GPU could be considered an example (except GPUs often have analogue circuitry as well to connect to monitors)

Application 1 and 2

- For the project, you are to attempt two versions of your application, namely:
- Application 1:
  - A baseline version (i.e. what you start with)
- Application 2:
  - An extended or enhanced version of application1 that has more functions or features (e.g. GUI) included.

Just to clarify: it is not really two different applications! It is rather a basic starting application that you attempt to make into a more complete application.

Consider application 1 worth 70% marks and application 2 the remaining 30% (i.e. increasingly high marks → increasingly more effort)

YODA Example and Scenario

- Delta modulator that grabs set of 8 bytes and outputs 1 byte
  - 128 | 200 | 220 | 201 | 201 | 201 | 127 | 108
  - => 100 = 01100100_2
- Application 1
  - Flash LEDs according to data send from PC
- Application 2
  - Perform delta compression on data sent from PC, send compressed steam back to PC

Decisions decisions … to use a GPU or FPGA for this? Application 1 sure would be more FPGA relevant, Application 2 looks more that a GPGPU could be a good option especially if it is just about the encryption happening on the same PC and being forwarded to one of its other (e.g. network) cards.

YODA Project Structure

#0 **(Form Groups)**

YODA Feature List
Due: 12-Apr 11:55pm

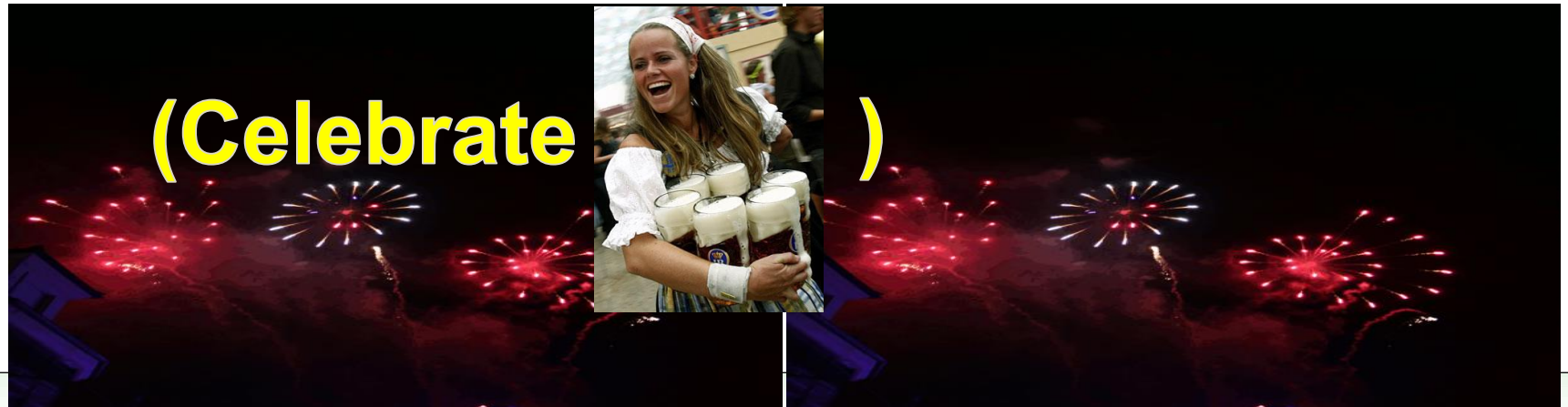
#1 **Blog**

#2 **Status Update**

#3 **Draft Paper (report)**

#4 **Demo & Acceptance Test (conference)**

#5 **Final Paper (report)**
& Code/Resource submission



Project Teams & Marking

- Projects done as teams of 4 or 3 members
  - (confirm other team sizes with lecturer)
- Milestone Dates – leading-up to 'YODA Conference'

Milestone 0: Group formed and topic Selection	**23 Mar**
Milestone 1: Proposal Blog	**12 Apr**
Milestone 2: Status Update * (need to schedule with your 'Team Manager')	**21 Apr**
Milestone 3: Draft paper	**28 Apr**
Milestone 4: Demo / Acceptance Test * (need to schedule with your 'Team Manager', team manager from other group attend too)	**8 – 12 May**
Milestone 5: Final Project Report and Code Repository Hand in	**15 May (final submit)**

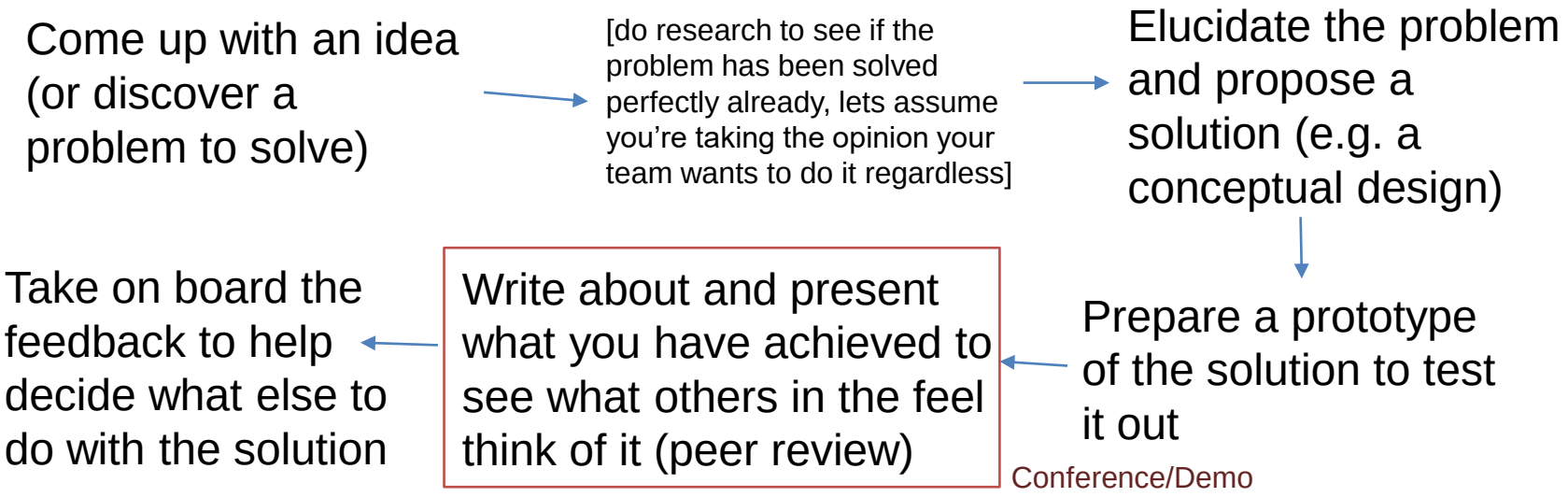
* Need to actually have something to show beyond just discussion of plans.

The 'YODA Demo/AT'* approach

*AT = Acceptance Test, used this year

- Why?
  - It is essentially planned around being a small scale experience of the typical 'R&D progress' …

The usual Research & Development process *(simplified)*…



Yoda Paper & 'Conference'

- The usual process is as follows.
- Prepare and submit an initial paper [in out case a draft]
  - Usually around 4-6 pages double column
  - Explain the solution, incl. some background.
  - Give sufficient explanation, but not too much detail
- Get feedback from reviewers [in our case, a team manager]
  - Reviewers give feedback on what they think, any aspects they found unclear, if it is it useful / sufficiently novel, appropriateness of topic for conference, etc.
- Revise the paper
  - Respond to reviewer requests
  - Submit revised paper + brief report describing responses made to reviewers' comments
- Present the paper [at an emulated conference]
  - Usually 8-15 minutes for an engineering conference presentation.
  - This larger audience (i.e. more than the reviewers) ask questions and give further insights beyond what was gained from the reviewers.

Project Teams & Marking

- Important: final report counts the most !
- Breakdown of marking

Milestone 0: Group formed and topic Selection	**0%**
Milestone 1: Proposal Blog	**5%**
Milestone 3: Status update *	**5%**
Milestone 4: Draft paper	**5%**
Milestone 5: Demonstration / Acceptance Test**	**20%**
Milestone 6: Final Project Report and Code Repository Hand in	**65%**

* May be more than one ‘status update’ which carries a small mark weight, as in sense and quality of teams response to queries during the project leading up to the main status update meeting.

** Would technically be Alpha Type Acceptance Testing, meaning it would largely have just the usual project team members, maybe some invited viewers / consultants too.

YODA Project counts 15% of course mark

YODA – Purpose

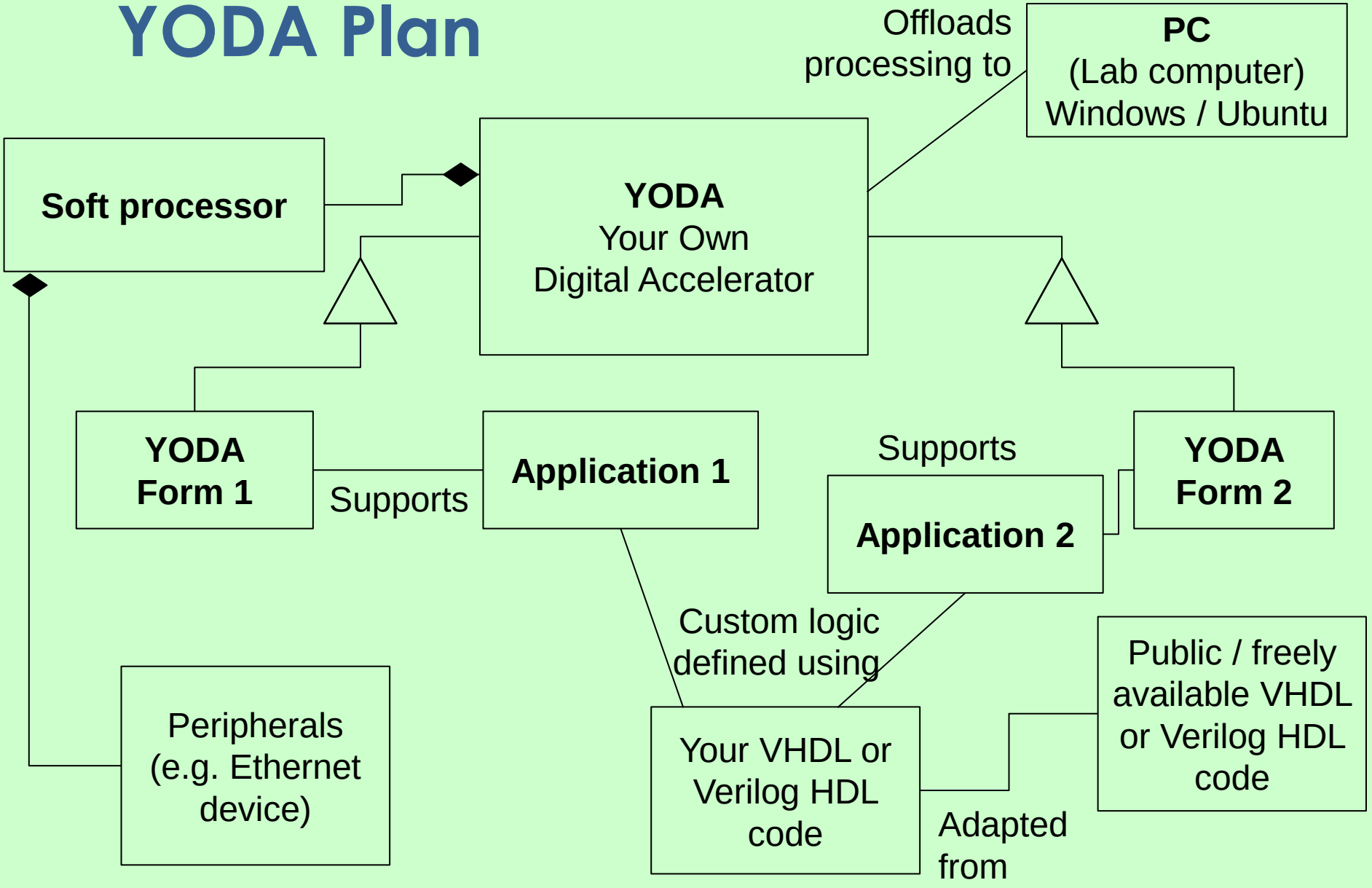
- At the end of the course you should have an understanding of how to developed an application accelerator for a PC using either
  - FPGA / FPGA-simulation and Xilinx-based development tools (and possibly evaluation board if using hardware)

  or
  - Good understanding of using FPGA simulation and means to tested simulated input and output

YODA Design Strategy

- In order to trial the reconfigurable aspect, your YODA prototype should support two applications
  - Application 1: something very simple (i.e., for testing your setup, send/receive data)
  - Application 2: more sophisticated / meaningful application (e.g., parallel pattern searches)

YODA Plan


Offloads processing to
PC
(Lab computer)
Windows / Ubuntu
Soft processor
YODA
Your Own
Digital Accelerator
YODA
Form 1
Supports
Application 1
Supports
Application 2
YODA
Form 2
Custom logic defined using
Peripherals (e.g. Ethernet device)
Your VHDL or Verilog HDL code
Adapted from
Public / freely available VHDL or Verilog HDL code

YODA
Option A or B
App 1 & 2

App 2 = All the bells and whistles, may not be sufficient time to do
App 1 = Backup / fall-back design more achievable in a short time

Let's see possible examples…

Example Scenario

App 2 = Music synthesizer that can play MIDI files (or similar type) and allows for multiple concurrent instruments, able to provide smooth sounds with a wide dynamic range.

FPGA Full Synth demo (A).mp4

App 1 = Music Beep Box, has a hard-coded tune sequence (stored in an array in BRAM) that specifies tone and duration. Can play one tone at a time.

FPGA Music Beep Box (B).mp4

YODA Presentation

- The presentation gives a clear impression of what was done
- You choose what to showcase (in the short time available)
- Should be close to the final version (the resources of which are submitted to provide evidence of having completed the work), but doesn't necessarily need to be the *final* final version.

YODA Report
('YODA conference paper')

- Use the paper template, and follow the guidelines for the sections (some flexibility in the headings)
- Introduction
  - Brief indication of background / context
  - Recap your topic and purpose of the solution
- Methodology
  - Procedure followed to design, implement and test the system
- Design
  - High level design
  - Finite State Machine (FSM) documenting your digital accelerator operation
  - Pseudo code (if relevant)
  - VHDL / Verilog snippets (indicating how your FSM was implemented)
- Experimentation and Testing procedure
- Conclusion and discussion (+ suggested future work, e.g. if another student group were to build upon the work next year)

What you need to do…

for the first two steps of the project

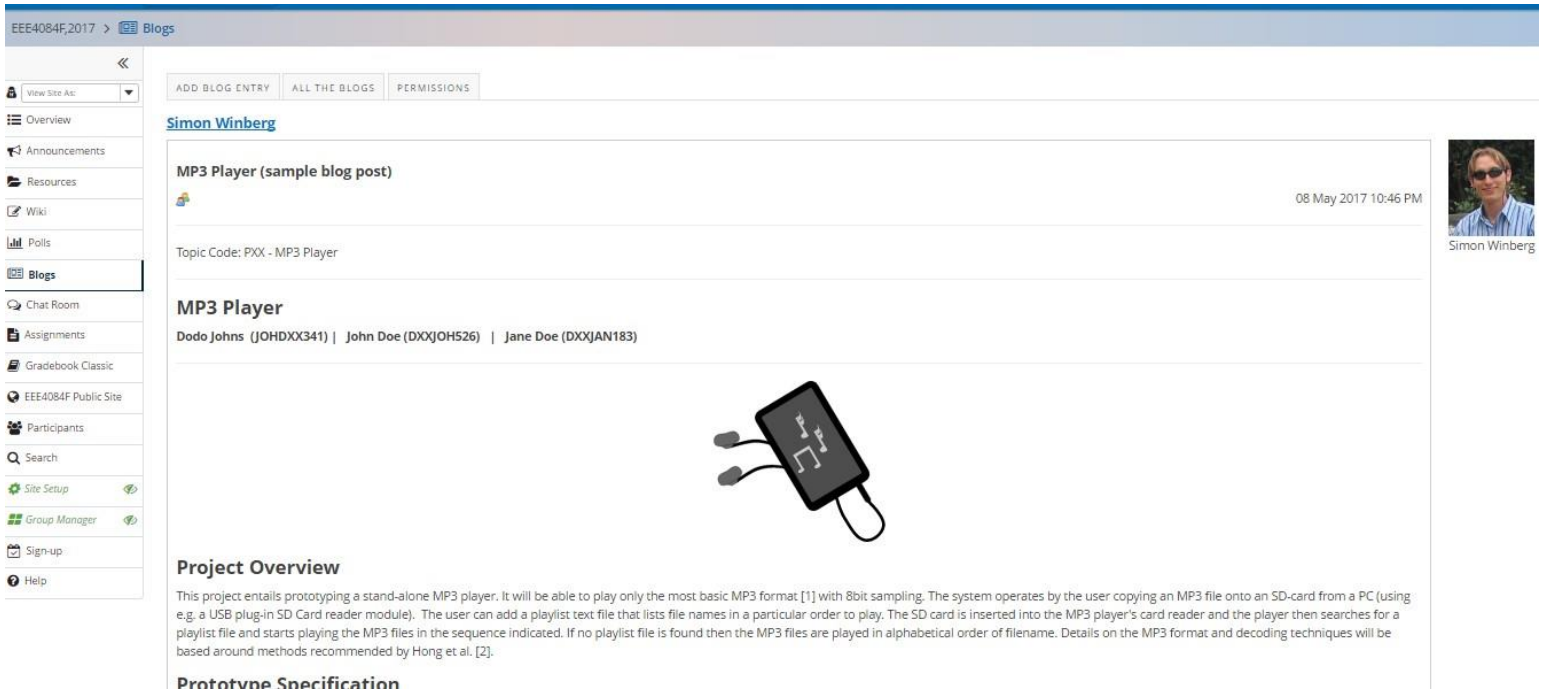
First step on the YODA project

Already done?!

- Please start trying to form a YODA team
- Teams need to be 4 members (i.e. two prac groups joined together)
- Don't need to choose a topic yet.. can start thinking about it in your teams
- Later on
  - If you've chosen your team, please update the YODA team list (Google sheet for this)
  - Can use the rest of the lecture to continue finding team mates or start discussing possible topics (you might need a smartphone/laptop to visit the website to facilitate this)

The second step – Milestone 1

Once you're formed a team you need to get together a conceptual design description and add a blog entry to the Vula site for this



Example of a blog entry showing what is needed

Conclusion of YODA Project Intro

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