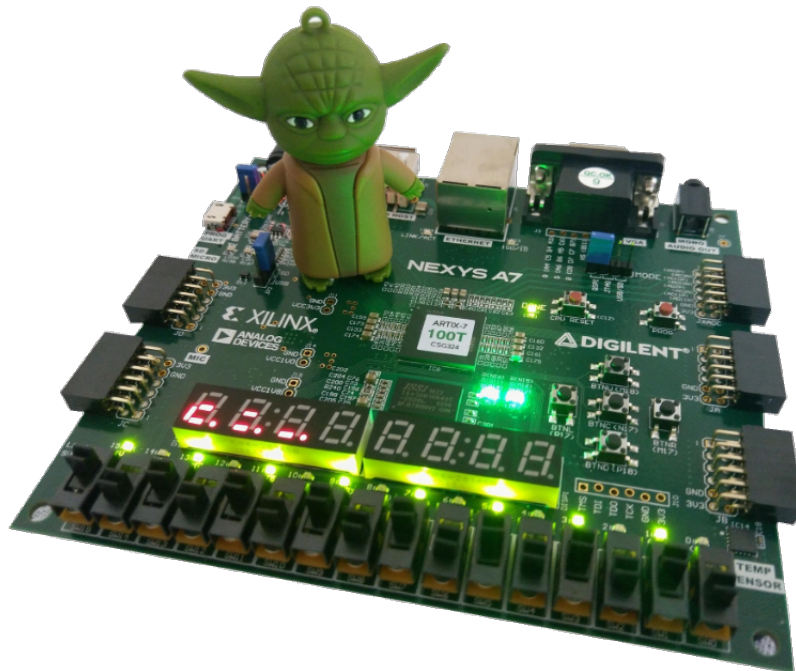


UNIVERSITY OF CAPE TOWN



EEE4120F

HIGH PERFORMANCE EMBEDDED SYSTEMS

YODA 2023

2 March 2023

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Milestone Overview

Please note that these dates are subject to change. For due dates, refer to assignments schedule on Amathuba.

Table I: The Milestone Overview for EEE4120F, 2022

Milestone	Description	Dates	Weight
Milestone 0	Group formed and topic Selection	23 March	0%
Milestone 1	Proposal Blog	12 April	5%
Milestone 2	Status Update	26 April	5%
Milestone 3	Draft Paper (not optional in 2023)	9 May	5%
Milestone 4	Demo / Acceptance Test*	8-12 May	20%
Milestone 5	Final Project Report and Code	19 May	65%

Introduction

Your Own Digital Accelerator (YODA) is designed to test your design and implementation ability when creating digital accelerators. A digital accelerator is a piece of hardware, often an expansion board or SoC chip, used to offload high-speed, or specialized, processing from the main CPU run. The operation performed by the digital accelerator can generally be represented by an algorithm, that could be implemented in software running on a host PC instead of (possibly much faster) on a suitable digital accelerator. Certain algorithms (not all of them!) can execute faster on specialized hardware than on a general-purpose CPU (such as an Intel processor).

This year, the YODA projects are expected to be based on FPGA or HDL development. Not using OpenCL or deploying processing on a GPGPU unless you are using OpenCL or CUDA together with an FPGA or HDL simulator. You do not necessarily need your digital accelerator to run on a physical FPGA (e.g. on a Nexys platform); you can make use of simulation to provide a proof of concept for the operations that would be deployed on a FPGA (or indeed on an alternate digital accelerator, such as fabricated on a co-processor chip if we had the facilities to do so). If you'd like to, you can make use of a GPGPU, in addition to HDL, to do for example demonstration of how fast an operation might run on the GPGPU, or as an additional part of your system.

Using an FPGA allows us to prototype hardware implementations of these algorithms and, possibly, providing a speed-up of these needed algorithms over execution of a software version on a general purpose CPU. This project experience is planned around mimicking a professional/academic experience whereby you develop a product (more the industry perspective), or conduct an research investigation (more the academic perspective), in which you implement the YODA project, and then you present it to the 'community' (simulated community of your classmates) at a conference. The project is structured in such a manner to be easy to follow through a set of deadlines, but will require effort to implement something worthy of the Hall of Fame (HoF), should you be interested in having your YODA project as a lingering legacy that may help inspire other learners in this and possibly other courses.

The HoF is a collection of the best projects for the year. The categories are Best Prototype, Best Report, and Best Concept. If you manage to enter into the HoF, your project will be added to the [HOF on the course website!](#)

1 Teams

Teams are planned around being a combination of two prac groups, implying the team size should be four students, an occasional smaller group would be permitted depending on the class size. If you need to formulate a team of a different size (e.g. to work on the project individually) then please notify the lecturer before starting on the project. Team of more than four members is not desired unless there is a mitigating reason for this (as it can imply an unfair amount of work in comparison to other teams, and students not getting adequate practical experiences). Regardless of the team size, the workload and distribution of this needs to be indicated to you 'team manager'; the workload and distribution of this may need to be adjusted so as to make this more consistent among the teams.

Each team will be assigned a team manager. This is someone who is not in the team, but rather a tutor, TA or lecturer who will act both as the manager and something of a consultant. Please be conscious of your "team manager's" time constraints - you can't bug them with many questions; you are meant to be largely responsible for your own development practices and problem-solving.

2 Milestones

The project is broken down into milestones, to better guide you through the project requirements. The following milestones are included in this project:

1. MS 0 - Team update
Details of who is in your team, and the project you've selected.
2. MS 1 - Proposal Blog
Consists of creating a blog outline, over viewing how you will approach the given topic.
3. MS 2 - Status update
Consists of an in-person meeting and a submission to Vula. The purpose of this meeting is to show progress of your implementation.
4. MS 3 - Draft paper
By this stage you should have started on the final submission paper, as it will assist you with time management and the conference presentation. This milestone counts for marks this year, to encourage students to start work on their reports earlier as the final report counts many marks (in prior years teams too frequently left report writing to the end of the project which resulted in sub-standard or incomplete reports).
5. MS 4 - Demo or Acceptance Test
A short demonstration of your system.
6. MS 5 - Final paper and code submission
The final hand in.

2.1 Milestone 0: Group Formation

To complete this milestone, your team leader will need to fill out a Google Form, which will be sent to you closer to the due date. On this form you will need to submit your team members and topic selection.

2.2 Milestone 1: Blog Proposal

For this milestone you will have to create a basic blog outline. The purpose of this milestone is to identify the key aspects of the project and what will be involved in the creation of your accelerator. Please refer to the rubric below on what you should include in the blog. Note that section 1 (previously mentioned in lecture ?? **lecture num TBD slide TBD**, as Application 1 or baseline application) refers the compulsory aspect of your topic and section 2 is the additional part of the topic. Consult the topics section of this document for further clarification on these sections.

Table II: Blog Proposal Rubric

Marking Category	Description	Section	Marks
Problem Description	Elaborate on what the YODA project entails and descriptions on the algorithms being implemented	Section 1	6
		section 2	4
Prototype Specification	Information on how you plan you create the accelerator and any specifications pertaining to this	Section 1	6
		section 2	4
Project Goals	The goals and aim of your accelerator.	Section 1	6
		section 2	4
References	Reliable and useful references		5
Total			35

2.3 Milestone 2: Status Update

You need to update your assigned team manager, i.e. the tutor or lecture to whom you have been assigned to report on your progress. This needs to be done in a short in-person meeting (or via online meeting), possibly with a follow-up where you post the substantiating evidence of your status report on Vula.

NB: upload supporting document, must provide:

1. Design document
 - (a) Block Diagram
 - (b) Schematic

- (c) Any alternate diagram such as statechart
- 2. Snippets of Code
- 3. Some initial simulation (if not real prototyping) results

You can add other things you think would demonstrate good progress and you can use your blog in the status update if it will help. The purpose of this milestone is to show progress that you are making on the YODA project. Please meet with your team manager or email your manager to provide an update of your progress. Mention at least 3x things that you have already done on the project (in terms of design work), 3x things that you are planning to do over the next couple of days (also design/implementation) and show some evidence of work done (if in person show on a PC or by email you can send screenshots of attached code files or figures). We will also award a quality of the work, for instance if your code is well structure and commented or your schematics well labelled you will get a higher value for the quality mark.

This is for marks.

Table III: Status Update

Description	Marks
Overview of progress	10
3x Things Done	5
3x Things to be done	5
Design document or explanation of your code/design so far	10
Evidence of work done (e.g. code snippet)	10
Overall quality	10
Total	50

2.4 Milestone 3: Draft Paper

For this milestone, you must submit a draft paper (in the IEEE conference format) to Vula. This is to show that you are making progress. You should have something to write for each part of the report through into to conclusion, but it obviously doesn't need to be fully complete, e.g. can indicate where you plan to put additional result images once you're done the needed tests.

This milestone does count for marks, it may likely improve your final report submission if you try to do a good effort on this draft report, adding references and the like to boost the quality. While you are encouraged to use the IEEE conference template for this milestone, that is not essential, you can use a standard template or Word / Google document for this. But for the final report you are expected to use the IEEE conference template.

2.5 Milestone 4: Demonstration and 'Conference'

The demonstration portion of the YODA project is a vital aspect of the project, as it provides the perfect opportunity to show how your accelerator works. You group will have to give an in person (or online) demonstration of your system to a Tutor, TA or Lecturer. This year it is planned to implement the 'YODA Conference' in which each group will do a 10minute presentation of their project showing results achieved thus far. The conference will happen during lecture periods. Each student needs to present in their conference presentation slot and need to be in two of the four periods in which the conference runs.

Table IV: FPGA Demo Rubric

Section	Description	Marks
Sec 1	Gold Standard Min Max Output	6
	FPGA Min Max Output	6
	Appropriate Speedup	6
	Read in Audio	6
	Clear Explanations	6
Sec 2	Gold Standard Min Max Interval Output	4
	Interval Min Max Outputs	4
	Appropriate Speedup	4
	Read in Audio	4
	Clear Explanations	4
Total		50

2.6 Milestone 5: Final Report and Code

This is the submission for the final YODA report. The YODA final submission counts for 65% of the project. The report counts 55% and the code/design repository counts 10%. Each category will be marked along the guidelines of the marking rubric. For example, if the abstract is fantastic and covers both section 1 and 2 points well then you will receive 6/6 for section 1 and 4/4 for section 2, resulting in a mark of 10 for the abstract. Whereas, if you cover section 1 points well in the abstract with no mention of section 2, your mark will be 6/6 for section 1 and 0/4 for section 2.

The rubric is broken down into 2 sections, where the compulsory section refers to the aspect of your chosen topic that is compulsory, this is the section that counts for 60% of your report mark and you have to pass this section to receive DP. The additional section counts for 40% of your report mark and is not required for DP. Therefore, in order to achieve DP you need 50% for section 1 only.

If your group attempts both section 1 and 2, which is highly recommended, consider writing one report that investigates the two different tasks. Therefore, your report should have aspects to each section within each heading. For example when discussing the background make points pertaining to both section 1 and 2. Furthermore, keep track of the number of points required for each section.

Table V: Final Report

Section	Description	Sec1: Marks	Sec2: Marks
Abstract	About 250 words, giving an overview of your project.	6	4
Introduction	A nice lead-in that states objectives and motivations clearly.	6	4
Background	Points supporting/leading to the motivation, some mention of literature or sources of information inspiration (textbooks and online repositories)	5	3
Methodology	How you proposed to go about building the system, some of which should have managed to do, but much of this may be hypothetical/recommended (i.e. if there was time, describe what you would do). Discuss how you would measure the results, and what measurements/metrics you would record, so there is a scientific grounding to your study.	6	4
Design	Elaborate on the design of the accelerator system and give thoughts on connecting up to a host. (note: methodology and design are not the same thing)	12	8
Proposed Development Strategy	This can be conceptual/something of a thought experiment. Discuss a bit as to, if this was a commercial product, what sort of supporting tools and framework would be needed to facilitate application development using this accelerator.	6	4
Planned Experimentation	Elaborating on the methodology, describe the experimental setup, how the experiments were implemented, e.g. commands performed. Could explain how golden measure would be used to compare accuracy of prototyped system (note results section shows the actual results, this just explains the experiments in more detail)	3	2
Results	Show your results (even if it's only golden measure testing).If you don't manage to get much results then add discussion about what would be anticipated were there time to do it (to run the proposed experiments discussed in the previous section), and if there is no time to complete experiments then provide model graphs providing an example of what type of performance / output / other results would be expected and an argument as to why you would expect these results.	12	8
Conclusion	Summarize the results collected. Were the objectives discussed in your design achieved? What else can be done to improve the system going forward?	6	4
References	References used in the report are from reputable sites/journal articles.	3	2
Code Repository Comments	Comments explaining the code in the git repository.	3	2
Code Repository Neat Code	Code is efficient and neatly coded up.	4	3
Total		72	48

3 Topics

This year the YODA projects are to be done using FPGA or at least HDL code for which part of your system will run on an FPGA or using a simulator. If using a simulator, there would understandably be some potentially manual intervention to get input from the host PC (or a simulated source of input data) into the simulated FPGA, and to get the results from the simulator and displayed or put into a visualization of the system output.

Each of these topics there will include two sections, Section One (previously mentioned in **lecture TBD!!**, slide 28 as Application 1 or baseline application) will be a more simple task that all groups will have to complete for 60% of your mark. Section Two will require your group to look into literature and implement your own algorithm for a specific task, which will have a weight of 40%. Furthermore, only section one is compulsory to achieve the DP requirement for completing the YODA project. Note, if you only attempt section one your groups maximum possible mark be 60%.

Example projects (these can be chosen) are shown below. The full list of topics for this year, the "YODA TOPICS" pdf will be available on the Amathuba course website. You are also welcome to propose your own topic, but do so in the first term.

Table VI: YODA Topics Examples

Topic	Section	Weight
Image Process	Sec 1: Median Filter	60%
	Sec 2: Edge Detection	40%
Sound Process	Sec 1: Min Max Amplitude	60%
	Sec 2: Interval Based Min Max	40%

3.1 Example Topic 1: Image Processing

3.1.1 Section 1: Median Filter

Median filtering is a common image processing operation, used to reduce noise. You would need to create a median filter that takes an image and then outputs the median filtered image. The algorithm you will have to implement is basic, where the outputted pixel value is the median pixel of the surrounding pixels as shown below.

Table VII: RGB Values

2,4,7	30,46,23	23,65,86
34,57,3	34,87,94	123,143,67
23,43,197	33,76,97	34,78,54

Table VIII: Sum RGB Values

13	99	174
94	215	333
263	206	166

Therefore, the median pixel will be 174. You will have to repeat this process with every pixel in the image.

3.1.2 Section 2: Edge Detection

Edge detection is an algorithm that is widely utilised in the field of computer vision. For this section of the YODA project you will have to look at literature and identify appropriate edge detection algorithms and implement one.

3.2 Example Topic 2: Sound Processing on an FPGA

3.2.1 Section 1: Min Max Amplitude

For this topic your group will have to program an FPGA to output the minimum and maximum value of an audio clip that is streamed into the FPGA. This topic can be implemented either on an FPGA or via simulation. However, if the simulation approach is taken, a very in-depth test bench has to be created in order to test the accelerator and virtual peripheral should be looked into.

3.2.2 Section 2: Interval Based Min Max Amplitude

Implement a program that will output the minimum and maximum value for an inputted interval length and audio clip. This means that a 10s audio clip where the set interval length input is 1s will have 20 outputs (min and max amplitude for each 1s interval). From these points you will then have to filter out all points that are 1 standard deviation from the mean. This filtering process has to be implemented for the max points and min points separately, resulting to two sets of outputs.