

EEE4120F Quiz 2 based on paper:

Hill and Marty "Amdahl's Law in the Multicore Era"

DATE: 09/3/2023

ANSWERS!!!

Please fill in name!

This is just a very short quiz, but it is for marks!

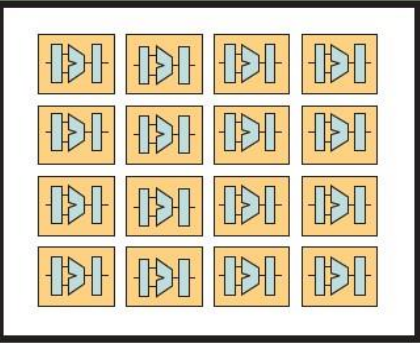
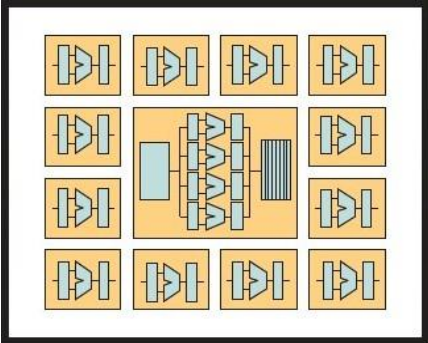
NB: Please select only one answer option for each question

CIRCLE/COLOR-IN ANSWERS FOR MULTIPLE CHOICE QUESTIONS

TOTAL NUMBER OF QUESTIONS : FOUR (4)

TIME (mins): 7

#	Question - EACH QUESTION WORTH 1 MARK	Sec	W	%	X
Q1	A major aspect, and indeed purpose discussed at the start, of this paper is about ...	60	2	11%	
	<p>[1] Pose an alternate perspective on the tensions between applications and software, which differs to the 'Golden Gate Bridge' scenario.</p> <p>[2] Encourage multicore designers to view the entire chip's performance rather than focusing on core efficiencies.</p> <p>[3] Provide a more optimized form of Amdahl's law for multicore processors.</p> <p>[4] Incorporate consideration for memory coupling to speedup analysis.</p> <p>[5] Discuss what is meant by a Compiled Binary Executable (or 'cbe').</p>				
Q2	The paper presents the concept of a BCE. Write out this acronym in full.	60	3	17%	
	Base Core Equivalent				
Q3	<p>The authors use variable r to represent how many resources, in terms of resources a single BCE needs, it takes to implement an enhanced multicore. They use the function $perf(r)$ to indicate the sequential performance of the enhanced multicore chip compared to a single BCE. In this question (which is an often-used simplification) you can consider $perf(r)$ to be the speedup of the enhanced multicore compared to one BCE.</p> <p>They say that while $perf(r) > r$ is maintained, dedicating more resources to the multicore suggests benefit, but at a stage when $perf(r) < r$ the addition of resources hurts parallel execution.</p> <p>Briefly try to explain more directly what they mean by this... why would there be benefit in dedicating more resources while $perf(r) > r$ continues. And why would it 'hurt parallel execution' if further enhancement causing $perf(r) < r$?</p>	90	3	17%	
	<p>while the $perf(r) > r$, this indicates that the speedup of the multicore enhanced processor design is performing better than that of r BCE cores working perfectly in parallel. This suggests that the design of the multicore is overall more efficient than r BCEs working in parallel perfectly without problems such as synchronization delays.</p> <p>when $perf(r) < r$ this indicates that the efficiency of the enhanced processor no longer achieves an equivalent parallelism performance of that of r BCEs, indeed that having used r BCEs resources to implement r BCEs would have given better performance than implementing the enhanced multicore which still uses equivalent resources but achieves worse performance. They do indicate that the enhanced multicore, when running sequential code, could still do that faster than one of the r BCEs</p>				

Q4	<p>Here are three mutlicore chip models, showing the arrangement of BCEs withing them (note that a mutlicore chip doesn't necessarily just use a collection of BCEs of the same design as the baseline BCE, it just indicates the equivelent resource usage). There are various models that Hill and Marty gave names to. Attempt to name the two multicore equivelents below according to the authors naming convention presented.</p>	90	5	28%
	<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="border: 1px solid black; padding: 5px; text-align: center;">  </div> <div style="border: 1px solid black; padding: 5px; text-align: center;">  </div> </div> <p>NAME: <u>Symmetric multicore</u> NAME: <u>asymmetric multicore</u> (with 16 one-BE cores) (with 1 4-BCE core and 12 1-BCE cores)</p>			
Q5	<p>The authors ended off with the concept of "Dynamic Multicore Chip"... besides suggesting that it would be nice if processor architects could have their cake and eat it. What do they mean by dynamic multicore?? What would be so great about such a thing? <i>PS: you could try such an experiment in a YODA topic if you wanted to ;-)</i></p>	90	5	28%
	<p>The suggestion is a multicore that could somehow dynamically swap between being a higher better-performance multicore and a set of equivelent BCEs. For example, when running sequential code it could be a 4-BCE, but when running parallel code swaps to a 4x 1-BCE processors.</p>			
	TOTAL :	390	18	100%
Time : time est. in sec W : Weighting of question % : How much question counts X : Office use				