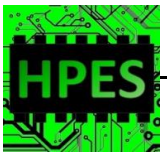


EEE4120F Quiz 2 based on paper:

Hill and Marty "Amdahl's Law in the Multicore Era" **DATE:** 09/3/2023

Name: _____ Student Number: _____ *Please fill in name!*

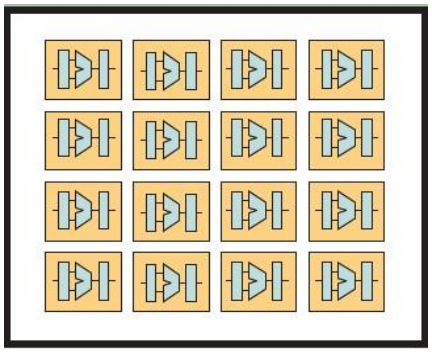
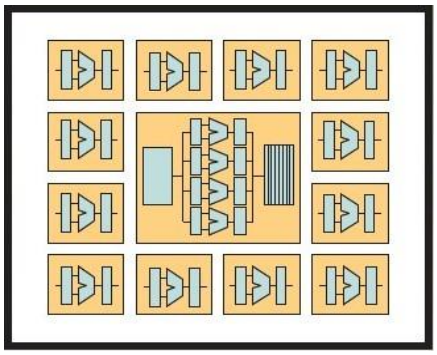
This is just a very short quiz, but it ***is*** *for marks!*

NB: Please select only one answer option for each question

CIRCLE/COLOR-IN ANSWERS FOR MULTIPLE CHIOCE QUESTIONS

TOTAL NUMBER OF QUESTIONS : FOUR (4) **TIME (mins):** 7

#	Question - EACH QUESTION WORTH 1 MARK	Sec	W	%	X
Q1	A major aspect, and indeed purpose discussed at the satrt, of this paper is about ...	60	2	10%	
	[1] Pose an alternate perspective on the tensions between applications and software, which differs to the 'Golden Gate Bridge' scenario. [2] Encourage multicore designers to view the entire chip's performance rather than focusing on core efficiencies. [3] Provide a more optimized form of Amdah's law for multicore processors. [4] Incorporate consideration for memory coupling to speedup analysis. [5] Discuss what is meant by a Compiled Binary Executable (or 'cbe').				
Q2	The paper presents the concept of a BCE. Write out this acronym in full.	60	3	15%	
Q3	The authors use variable ***r*** to represent how many resources, in terms of resources a sngle BCE needs, it takes to implement a enhanced multicore. They use the function ***perf(r)*** to indicate the sequential performance of the enhanced multicore chip compared to a single BCE. In this question (which is an often-used simplification) you can consider ***perf(r)*** to be the speedup of the enhanced multicore compared to one BCE. They say that while ***perf(r) > r*** is maintained, dedicating more resources to the multicore suggests benefit, but at a stage when ***perf(r) < r*** the addition of resources hurts parallel executation. Briefly try to explain more directly what they mean by this... why would there be benefit in dedicating more resources while ***perf(r) > r*** continues. And why would it 'hurt parallel execution' if further enhancement causing ***perf(r) < r*** ?	90	5	25%	

Q4	Here are three mutlicore chip models, showing the arrangement of BCEs withing them (note that a mutlcore chip doesn't necessarily just use a collection of BCEs of the same design as the baseline BCE, it just indicates the equivelent resource usage). There are various models that Hill and Marty gave names to. Attempt to name the two multicore equivelents below according to the authors naming convention presented.	90	5	25%	
	  NAME: _____ NAME: _____				
Q5	The authors ended off with the concept of "Dynamic Multicore Chip"… besides suggesting that it would be nice if processor architects could have their cake and eat it. What do they mean by dynamic multicore?? What would be so great about such a thing? *PS:* you could try such an experiment in a YODA topic if you wanted to ;-)	90	5	25%	
	TOTAL :	**390**	**20**	**100%**	
	Time : time est. in sec W : Weighting of question % : How much question counts	X : Office use			

Extra space if need: