High Performance Embedded Systems EEE4120F

FINAL EXAM

MEMO

PART C – Short Answers

10 July 2020

2 hours

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Notes on assessment of independent work that was originally allocated towards the final exam, however due to transitioning to distance learning and no longer having a closed examination have been changed to the following:

Part A is an online multiple-choice test, the answers of which were included in the printout of the question in "EEE4120F - Exam Questions - Part A (multiple choice).pdf"

Part B is part of the GA2 Assessment, this is an assignment, there is no memo but rather the students response to the tasks provided will be assessed in terms of applying their scientific and engineering skills to solve a representative problem.

Part C (this part of the assessment) involves a set of short written responses that may include a limited amount of coding or code snippets and are used to assess the students competencies in general development skills concerned in this course. A Marking Memo is provided rather than a specific solution as there are many potential ways to respond to the issue posed.

Part C: Short Answers [50 marks]

Marking guidelines:

Part of the purpose was to give the student a non-trivial design to consider, drawing on their understanding of interpreting digital design schematics and explanations of interfacing and handshaking protocols in order to effectively respond to the problem posed.

Marking comments are provided below the questions in red.

Question 1 [40 marks]

Please answer these sub-questions that relate to the design on the previous page …

(a) Based on the given design, would you say that the CMP components of this design are synchronous or asynchronous? Briefly motivate your answer. [4 marks]

The student should realized from the description that we are talking about a synchronous design for the CMP because it will be clocked.

(b) Consider the CMP component of this design. In order to better understand its operation, and particularly if we wanted to compare it to a Verilog equivalent, you are asked to develop a C version for this component. Accordingly, provide a C function to imitates the operation of this component. Add to your answer an explanation of what ports you think the CMP component should have and how you have emulated these ports, or emulating input changes, in C [15 marks].

Multiple Zoom lectures were dedicated to helping student understand how to develop an initial executable model in C or Python in order to develop an understanding of a problem and potential ways to solve it using the more hardware-centric approach of input / output signals and busses. The students have shown varied levels of success in using this approach, but it is certainly an effective means for them to gain good confidence on whether or not a solution is right, particularly if they are working in isolation without the advantage of prac partners and tutors to help them solidify their understanding and gain confidence. Things of importance in this C solution: are consequentially, naming the outputs appropriately, possibly just having a a>b output since the other outputs are not used in this system. The a and b inputs should be specified as unsigned char to mimic 8-bit buses. A clk input should be given, and treated as a binary value; although it can be specified as an int and testing if e.g. the previous value was less than the current value to detect a positive edge. The function should rather have a variable parameter for a>b instead of returning a function. Furthermore, in accordance with the design of the CMP, it should wait for 'Tol' clk pulses to pass before changing the a>b output that connects to Trigger, and then reset the wait time so as to slow down the speed at which the outputs change. A portion of 4 marks will be added to neatness and use of comments.

(c) Now implementation the CMP component as an actual Verilog module, you could call it cmp.v. Note you are not required to implement a testbench (see (d) below). [15 marks]
(*Hint:* Appendix A gives a Verilog cheat sheet.)

As per the description above, the student needs to make allowance for clk and the development of a state machine so as to slow down the rate at which the outputs are responded to in terms of input changes. Marks will be awarded to the interface description, busses of the correct side, internal registers (e.g. a counter to manage the Tol aspect). A portion of 4 marks will be added to neatness and use of comments.

(d) Discuss how you could go about implementing a test bench for the CMP component that you have implemented. Note that *you are not* required to implement a testbench, however you can include code snippets to help illustrate you answer. It is important that plans for the testbench would be sufficiently thorough considering the important operational characteristics of the CMP component as explained in the design description. [6 marks]

The student is nor required to provide a full testbench but rather to discuss channelges that may be involved with building one, such as how to simulate a clock running at 10MHz and delays of TOL ms.

Question 2 [10 marks]

Marking guidelines: likely responses are discussed below the sub-questions.

A generally desirable aspect of a dynamically reconfigurable system is having aspects of the design that can fit on a single slice, so that just that slide can be reprogrammed without having to spend more time reprogramming other slices in the design. Some of the sub-questions below relate to the design on the previous page.

(a) What are potentially limiting factors on deciding whether or not a design, such as the design given on the previous page, would be able to fit into a single slice? [3 marks]

A major factor will the be limitation of interconnects between modules and the amount of memory that a module might need to use.

(b) If you had recently given a client your BOM (i.e. bill of materials) for the dual sensor monitor system, and he had come back to you with a complaint, saying that he had found on the web a PLD that costs just $2, which could replace the FPGA you proposed and thereby much reduce the cost. Considering that part of the requirement is it being dynamically scalable to over 5 simultaneous, what would your response be to motivate for sticking with an FPGA? [4 marks]

A major factor will the issue of scalability as well as the complexity of the design. If it were a CPLD that the client had found and consider using, there may be more purpose for thus; but a CPLD is unlikely to be as cheap as $2, it is likely to close closer to, probably at best $30 depending on the order volume… which is not necessariy going to be much cheaper than a low-cost FPGA which would probably be in much excess to what this particular problem needs, but compared to a basic PLD it would still support a significant amount of scalability for this system.

(c) Comment on the potential benefits that may be achieved by doing simulation of an Verilog or other HDL design rather than diving in to trying to get it working on hardware first (you could refer to a design concept, such as the design concept on the previous page, to use if needed as an example to aid your explanation). [3 marks]

The benefit of simulation is, for-more in the development of a new module, to establish a good understanding of what the module is doing, at least in terms of small tests, e.g. running short sequences of test vectors and developing assurance that those are being handled properly. If one were using hardware and skipping simulation, these type of small tests are assuredly also the fist type of tests that would be run on the system – however in the case of hardware it would likely be a much longer process, needing to establish means to view the results of the tests, possibly running tools like ChipScope monitor pins. The code-test-debug type of cycle is consequently likely to be much lengthier than the case for simulation. However, at some point it will become necessary to transition from relying on simulation towards running on hardware – but simulation is likely to get to a stage where more substantive testing can be done sooner on the hardware and thusly speedup the performance, and likely quality, of the project overall.

END OF PART C EXAMINATION