EEE4120F,2020 > Tests & Quizzes

NOTE: The correct answer is indicated indicate,
see 'Answer Key' below the answer options.

Tests & Quizzes

Assessments | Question Pools | Event Log | User Activity Report

Questions: EEE4120F 2020 - Exam PartA

10 Existing Questions - 50 total points

Add Part | Preview | Print | Settings | Publish

Part 1 Default - 10 questions Copy to Pool | Edit

Add Question select a question type

Question 1 Single Correct - 5.0 points Remove | Edit

Given the following Verilog code... how much slower is sclk than clk? Choose the most correct answer below.

```
module slowdown (clk, reset, sclk);
 // define the IO ports for this module
 input  clk, reset;
 output reg sclk;

 // define internal registers
 reg [2:0] cnt;
 // trigged based to input lines...
 always@ (posedge reset or posedge clk or negedge clk)
  begin
   if (reset == 1'b1) begin
     sclk <= 0;
     cnt<= 0;
    end
    else begin
     cnt = cnt + 1;
     if (cnt == 3) begin
       cnt <= 0;
       sclk <= ~sclk;
     end
    end
  end // always@
endmodule
```

A. sclk would be 1/6 of clk

B. sclk would be between 1/4 and 1/5 of clk

C. sclk would be 1/3 of clk

D. sclk would be 1/2 of clk

Answer Key: C
Incorrect Feedback:
Obviously slows by 1/3 because every 3rd edge of clk is an edge in sclk.

Question 2 Single Correct - 5.0 points Remove | Edit

Consider two program solutions: one that is sequential and the other that is parallel. If it is found that the sequential operations takes 2 minutes and 15s from launching the program to finish, but the parallel version takes 2s to startup before the nodes are ready and another 20s to complete operations including collation and presentation of the results... what can we say about the speed-up of the parallel over the sequential version? (Select the most correct answer below.)

A. This is a pretty decent boosting of the process, achieving a speed-up of over 6!

B. It's a speed-up factor of 135/(135+22) or 113s performance improvement giving a total speed-up of 85%.

C. It is not possible to draw any remotely accurate conclusion from the limited information provided.

D. In order to complete a speed-up calculation, even using the basic version of Amdahl's Law, it is necessary to know the volume of data concerned in relation to the processing performed. Accordingly, if the data used in this case was N elements, it can be extrapolated the speedup will be [135/(135+22)] for N; thereby we can say for M elements the speedup factor will be [135/(135+22)]*M/N.

Answer Key: A
Incorrect Feedback: speedup = T_org / T_new where T_org is the time of the original program for which you are calculating the speedup of the new program that took T_new to run the same problem.

Question 3 Single Correct - 5.0 points Remove | Edit

In order to calculate the 'Total Latency' of a communication channel, it is necessary to consider a number of characteristics that influence communication on this channel. Select which one of the options below has the most relevant aspects that need to be known in order to calculate total latency of the channel. (Select only one option)

A. Time of flight; Send overhead; transmission time;

B. Transmission duration; Receiver overhead; Time of flight; Send overhead.

C. Communications sending overhead (including things like error-correcting codes); Data transfer time; Time of flight duration.

D. Transmission time; Time of flight; Receive time

Answer Key: B

Question 4 Single Correct - 5.0 points Remove | Edit

Select the best choice below that describes a "Golden Measure" in relation to how it is used in this course and for taking about HPES system design.

A. A Golden Measure is a lot like Golden Syrup (if you have a sweet tooth); it's sweet and delightful, it runs smoothly, needs very little hassle to get the right data set up and tested, and it usually has a nice GUI.

B. A Golden Measure is rather like a lead balloon. It's basically something that is unwieldy, takes ages to get results from, and is likely to be unresponsive and give uncertain results... but this doesn't mean to say, like a lead balloon, that if you don't fuss over it and give it lots of hot air, it still won't work.

C. A Golden Measure is more like a star football player. As the 'golden' part of the name suggests, it's going to cost you - not as much as Lionel Messi (Si amigo. ¡Mucho dinero!) - but on the upside, like Messi, it will give you fantastic performance, and that is what you are wanting from a Golden Measure.

D. A Golden Measure is more like a boring brick of a solution - it may likely be slow and heavy on the resources, it might not be well optimized, and it might not have a fantastic GUI to show results; but despite its limitations, you're confident that it gives correct results.

Answer Key: D
Incorrect Feedback: A Golden Measure might look as exciting as an old brick, but what you want it to deliver is a very accurate and trustworthy result.

Question 5 Single Correct - 5.0 points Remove | Edit

There are a number of reasons - and items - that one might benchmark; indeed if you look up the definition of benchmarking it states: "Benchmark: a standard or point of reference against which things may be compared" (Oxford English Language Dictionary). So, for example, when benchmarking a computer you might choose a benchmark of a 20" screen being the baseline for which you are going to measure other options; indeed your purpose might not just be performance. However... when we are talking the development of a high performance computing or HPES application solution, what are the main objectives of our benchmarking? (excluding cost here, because cost optimization is often a major development goal aspect that is benchmarked at least in the design phase).

A. The main objective of benchmarking HPES systems is comparing their size, power and bandwidth utilization.

B. The main objective of benchmarking HPES systems is comparing their speed, power and resource utilization.

C. The main objective of benchmarking HPES systems is comparing their power utilization, network utilization, and operational utilization.

D. The main objective of benchmarking HPES systems is comparing their speed, communications, and correctness.

Answer Key: B

Question 6 Single Correct - 5.0 points Remove | Edit

Which one the following statements most accurately defines the concept of 'wall clock time' in relation to HPES systems as discussed in lectures?

A. Wall clock time is equivalent to performance in real-time, it gives a very accurate impression of the performance, where a measured result of e.g. 1s, corresponds extremely close to a time of 1s in the real world.

B. Wall clock time is usually, at best, a subjective impression of the performance - borrowing its name from how a wall clock can often be so incorrect So, it is refers to the fairly loose talk by developers concerning their impression of the performance of a system; e.g. Dilbert might say to Wally, "your report says your widget take 30s to give a result, but your wallclock timing must be rubbish because on mine it reports 1h"; Wally: "Maybe so, but I fixed Boss's walk clock to be fixed permanently at 5pm so he'll probably tick the 'good' boxes on this one."

C. Wall clock time is highly accurate, alluding to high precision and timing everything; while the

timing is based around execution levels, such as system time, it reports on the total time in either physical or simulation time (in the fine resolution down to propagation delays) consumed by the critical sections of the application.

D. The term "Wall clock time" is used specifically to state that the timing is being done by a means outside the computer system being measured.

Answer Key: A

Question 7 Single Correct - 5.0 points Remove | Edit

Which one of the options below IS INCORRECT concerning a von Neumann computer... (select only one option that is incorrect)

A. The von Neumann computer has RAM memory that stores both programs and data.

B. The von Neumann computer design cannot really be called an archaic and irrelevant design concept that has no relevance to any of today's computer system designs.

C. A von Neumann computer was originally programmed by hard-wiring the instructions; but more recently these were placed in dedicated instruction memory that was loaded into the CPU.

D. The earlier A von Neumann computers had simple ALUs, which would do basic arithmetic operations such as ADD, but would have excluded something as complex as a multiply or divide circuit.

Answer Key: C

Question 8 Single Correct - 5.0 points Remove | Edit

This question concerns MPI vs. OpenMP. One of the statements below IS FALSE concerning MPI and/or OpenMP. Which statement is false? (choose only one option.)

A. MPI standards for 'Message Passing Interface' whereas OpenMP stands for 'Open MultiProcessing'. Both are useful for developing parallel programs.

B. A drawback to MPI is that it is not fully consistent with standard C or C++, but instead utilizes a number of 'embellishments', particularly pragmas, that are needed for implementing parallel solutions.

C. MPI is specifically designed around applications running on different PCs being able to communicate with each other, rather than being focused on applications running on a single PC being able to communicate with each other.

D. The programs that are involved in an MPI-based solution do not have to all be compiled by the same compiler.

Answer Key: B

Question 9 Single Correct - 5.0 points Remove | Edit

Assuming that a is defined as a bus of 8 wire in Verilog (i.e., wire [0:7] a;) then which of the following statements will save the value 1 (i.e. 0x01) in this bus?

A. a <= 8'b1;

B. a = 8'b1;

C. a = 8'h01;

D. None of them if 'a' is just a wire that doesn't connect to storage... or all of these if 'a' connects to something that will store data.

Answer Key: D

Question 10 Single Correct - 5.0 points Remove | Edit

A clock buffer is an important feature that is needed in large designs. What is the main reason for using clock buffers?

(•) A. A clock buffer can be considered as a type of current amplifier, working somewhat like a transistor in a circuit that amplifies a weak input signal.

( ) B. A clock buffer is predominantly a clock slew corrector. As you get deeper into a combinational logic design, it corrects for the propagation delay of getting the clock signal to where it is needed.

( ) C. A clock buffer is effectively just another name for a global buffer or unit delay. It holds the data for up to a few microseconds before becoming invalid (x in simulation).

( ) D. A clock buffer is like a SR flip-flop, it allows the circuitry connected after the clock buffer to be isolated from further changes in clock, the clock gets rejoined once the circuitry using that clock reenables the buffer for responding to the clock.

Answer Key: A

Add Question select a question type

Update Points Update Order

Change Profile Picture

Error removing image
Error uploading image
Upload Choose file No file chosen

Save Cancel Connections ✖ Remove

Search for people ...
View More

My Connections | Pending Connections

You don't have any connnections yet. Search for people above to get started.
You have no pending connections.
←Back to My Connections
Search for people ...
$({cmLoader.getString("connection_manager_no_results")}

Done