EEE4084F Quiz 3: Lectures 12-16; CH 7, 14

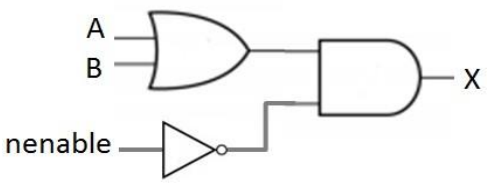
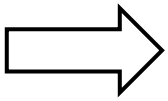
25-Apr-13

This quiz is for marks! Maximum recordable mark is 100%.

PLEASE ANSWER ON A SEPARATE PAGE / IN ANSWER BOOKLET

MAKE SURE YOUR STUDENT NUMBER IS ON YOUR ANSWER BOOK

TOTAL NUMBER OF QUESTIONS : SIX

#	Question	Marks
Q1	This question and the next relates to CH7 of the textbook. (a) An ideal transfer function is used in describing performance criteria of an ADC. Explain what is meant by the ideal transfer function and provide an example of one with reference to the operation of an ideal 2-bit ADC, assuming the ADC operates on input voltage *x(t)* in range -1V to 1V DC. Indicate on your diagram whether you are using the mid-riser or mid-thread convention. [6 marks] (b) The offset error is a static metric that describes the operation of an ADC. Explain in reference to an ideal transfer function what is meant by the offset error and how a 'trimming resistor' can be utilized to compensate for this error. [4 marks]	10
Q2	In terms of ADCs, the quantization-noise-ratio (or SNR_{quant}) is approximated as follows: $SNR_{quant} = (1.76 + 6.02N)$ dB where N = number of bits of resolution (a) If the signal to noise including distortion ratio (SNDR) of an 10-bit ADC is found to be 44dB for a particular hardware platform, then what is the actual number of effective bits of the ADC in this (probably poorly designed) system? [4 marks] (b) Briefly explain how a flash ADC operates, provide a *simple block diagram* to illustrate your description (you can refer to parts of the diagram in your text; you can use a simple 2-bit ADC to limit the size of the diagram). [6 marks]	10
Q3	This question relates to CH14. (a) What is the difference between a binary fat tree and a binary tree network? Provide a generalized discussion that relates to the root (R), parent (P) and child (C) switches and processor nodes (PN). [6 marks] (b) Indicate the scalability implications of a binary fat tree. [2 marks]	8
Q4	(a) Discuss two drawbacks and two advantages of using FPGA, as apposed to a more traditional microcontroller/microprocessor based approach for the development of embedded systems. [4 marks] (b) What is the benefit of using an HDL for designing ASICs or FPGA implementations instead of using the schematic or block diagram editor that is included with tools used for this type of development, such as Quartus II. [2 marks] (c) What is the difference between the *synthesis step* and the *place and route* step in the sequence of FPGA bitfile generation stages. [2 marks]	8
Q5	(a) Explain what a digital application accelerator is. Provide an example of such a product (you can use your own creativity for this one if you like.) [4 marks] (b) Provide the implementation of a Verilog module that represents the combination logic circuit shown below right. A starting point (that you don't have to reproduce in your answer book) is given on the left. [6 marks] module mycircuit (X,A,B,nenable); ... your code code will be put here ... endmodule 	10
	 *… please turn over for some multiple choice questions…*	

Q6	These are multiple choice questions. Select only one answer for each. [2 marks each] (a) The Stratix is the high-end FPGA family for which brand of FPGA manufacturer? (i) Xilinx (ii) Actel (iii) Altera (iv) Lattice (v) Achronix (b) Of the various FPGA manufactuers out there, which one is focused on being the market leader in very high speed (but not necessarily high capacity) FPGA chips? (i) Xilinx (ii) Actel (iii) Altera (iv) Lattice (v) Achronix (c) The greatest challenge that reconfigurable computing application developers face nowadays is: (i) Learning how to make the barebones platform into a useful and usable computer. (ii) Drawing circuit diagrams for reconfigurable computer designs. (iii) Finding the correct tools for generating bitfiles to program reconfigurable computers. (iv) Choosing appropriate interfaces to connect to a host computer. (v) Programming in C (d) Assuming a, b and c are all wires in Verilog. Consider the command bufif1(a,b,c). If b and c are both set to 0, then what is the value of c? (i) c=0 (ii) c=1 (iii) c=x (iv) c=z (v) c=L (vi) c=H	8
	TOTAL :	54