# EEE4084F  Quiz2 Sample Solutions                    2013

Q1.

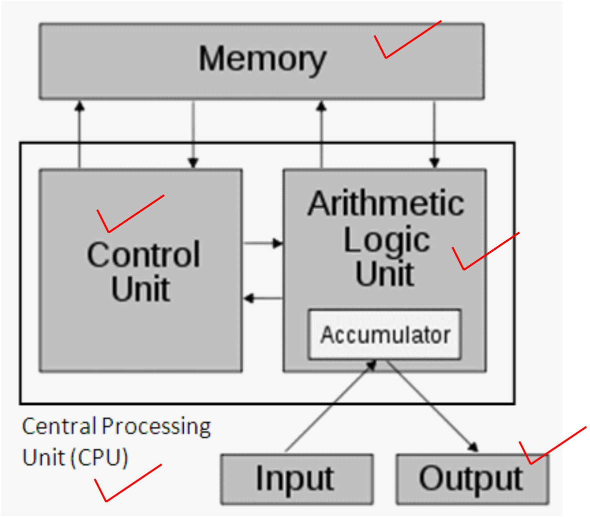


Figure 1: The Von Neumann architecture

5 marks

Q2.

SISD: Single Instruction Single Data

SIMD: Single Instruction Multiple Data

MISD: Multiple Instructions Single Data

MIMD: Multiple Instructions Multiple Data

1 x 4 marks each = 4 marks

Q3.

(a) **Uniform Access** = each processor connected directory to memory, each processor has the identical access permissions and access times to the memory.
**Non-uniform access** = not all processors in a multiprocessor system have the same access times and permissions to memory. Access to memory between processor groups is slower than access to memory directly coupled to a local processor group. [2]

(b) The processors in a SMP architecture are of the same type with the same connection to memory, following a symmetrical approach. For simplification of the design and of compilers to generate the code, it will be advantageous for the processors to all access memory in the same way, meaning that the same code can run on either one of the processors in the system, which is achievable using the uniform access approach. [4]

(c) Disadvantages:
- Lack of scalability between memory and number of CPUs.
- Adding CPUs can increases traffic on shared memory-CPU path.
- Programmer responsible for implementing/using synchronization constructs to ensure correct access of global memory.
- Becomes more difficult and expensive to design and construct shared memory machines with ever increasing numbers of processors. [2]

[8 marks]

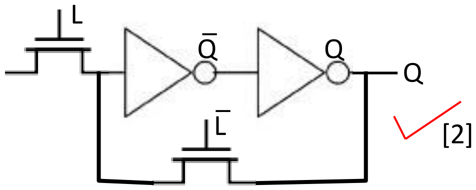
Q4.

(a) iv
(b) ii
(c) True/false answers:
    i. T
    ii. F
    iii. F
(d) ii

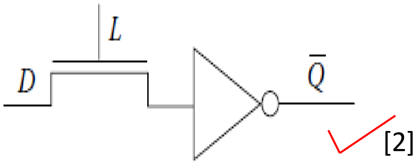
[2 marks each x 4 = 8 marks]

Q5.

(a) Static logic holds its output indefinitely while voltage is applied (the internal memory state doesn't decay unless the voltage is removed). Dynamic logic output is stored as capacitance, and decays with time, whether a voltage is applied to the circuit, unless the memory state is periodically refreshed (i.e., reinforcing/rewriting the stored charge). Dynamic logic circuits are usually smaller as the illustration below suggests. [4]



Structure of a static CMOS logic, showing a larch



Dynamic CMOS logic showing a latch

Dynamic logic is faster, considering use of nMOS transistors and smaller input load capacitance. The transistor count is about half (on average) compared to static logic, which can imply less transitions for each change of state (essentially in the case of long activation chains). [2]

[10 marks]

Q6.

(a) Functional decomposition separates the solution/problem into a collection of different computation tasks, some of which may be done in parallel with others. Domain decomposition separates the *data* into smaller chunks that are fed to parts of the solution or the same solution run in parallel on different chunks (the same chunk may also be used simultaneously by different tasks implementing part of the overall solution). [4]
(b) The new pixel colour for each pixel is dependent only on its close neighbours. The same exact operation (with the possible exception of pixels on the edge) is applied to each pixel. Since the blur operation itself is dependent on all its neighbouring pixels, the operation cannot be effective separated into smaller parallel parts. Therefore there is little merit in performing functional decomposition; however the problem is very much appropriate for domain decomposition considering that each pixel has so few dependencies on other pixels. [2]
(c) It is a course grained problem as there is little data dependence; each pixel value is only depends on the original value of its nearest neighbours, i.e. the new blurred value for the nearest neighbour pixels is not used. [2]

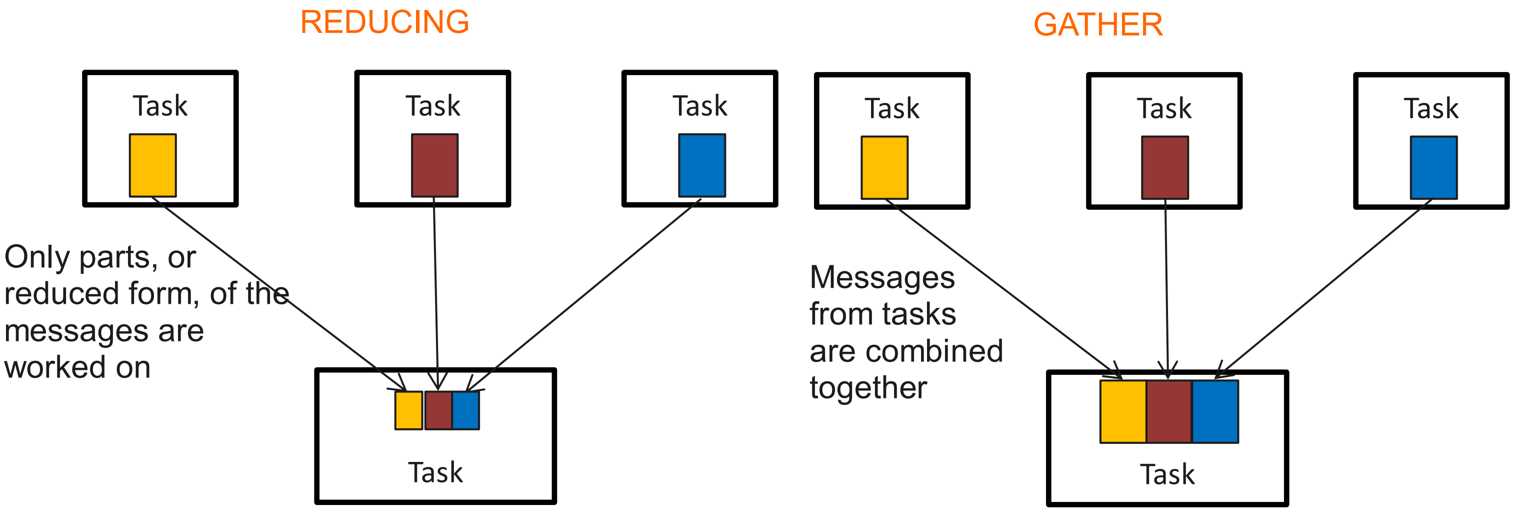
[8 marks]

Q7.

(a) Bandwidth = amount of data that can be sent per unit of time. Usually expressed as megabytes/sec or gigabytes/sec. [2]

(b) Highly visible [2]

(c) Reduce pattern = each task sends only part, or a reduced form, of its results to the master node collecting results (see diagram on left below). i.e. the cutting down/optimization of results is done by the source.
Gather pattern = each task sends the whole set of its results to the node collecting results (see diagram on right below). i.e. cutting down/optimization of results done by the target. [4]


REDUCING
Task
Task
Task
Only parts, or reduced form, of the messages are worked on
Task
GATHER
Task
Task
Task
Messages from tasks are combined together
Task

[8 marks]

Q8.

(a) All the tasks need to reach a marked point before they can all continue on after that point.

(b) Load balancing is a process that attempts to distributing work among tasks so that all tasks are kept busy most of the time.

(c) Verification = "Are we building the product right?" Have we made what we understood we wanted to make? Does the product satisfy its specifications?
Validation = "Are we building the right product?" Does the product satisfy the users' requirements. Remember: Verification before validation (except in duress).

[2 marks each x 4 = 8 marks]