EEE4084F: Digital Systems

10 May 2012

Quiz 4

Lectures 15,16,18, 19; Seminar 7: Ch 24 pp. 463 - 469

Time: 45 minutes 45 marks

NB Please answer Question 1 on a separate page.

You can answer Questions 2-3 together on the same page.

Question 1 [12 marks] *IMPORTANT:* try to answer this question as it relates to ECSA requirements.

This question relates to the Yoda Blog.

(a) Briefly describe the problem your YODA project concerns and outline the solution. [4 marks]

Questions 1 (b) and 1 (c) relate to the following system description:

Consider that you want to develop a high speed delta modulation module. A delta modulator, as you may be aware, receives an N-bit input (e.g., a 8-bit byte) and outputs a 1-bit value to say if the current input is smaller (by outputting a 0) or greater (by outputting a 1) than the previous value received. For example, if the system is initialized to assume the last value was 0, then the sequence of bytes 100, 101, 102, 99 would output the sequence of bits 1, 1, 1, 0. The input words are coming in at M words per second; the output delta modulation bit needs to be produced at the equivalent rate, but a slight delay in the calculation is acceptable.

Answer the following:

(b) In the delta modulation module describe above, think of at least two design questions that you would need to answer in order to implement this module. [2x2= 4 marks]

(*Hint:* a design question, as the term suggests, is something that is not explicitly specified in the requirements, which you need to answer or decide a solution for in order to have a better understanding of how to design and implement the system concerned.)

(c) Identify two criteria of a suitable solution for the delta modulator. [2x2 = 4 marks]

(*Hint:* question (c) is intentionally an open-ended question; you need to draw on your expertise in computer engineering theory to suggest suitable criteria based on the limited information give in the description above.)

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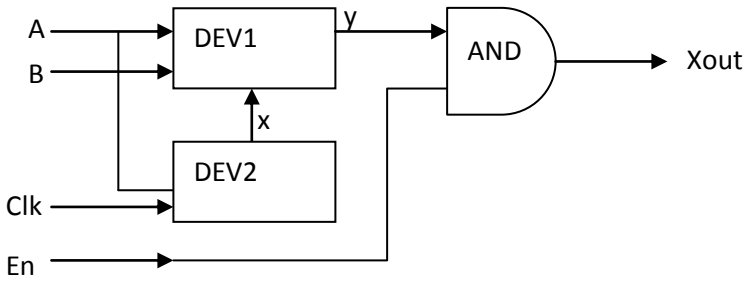
Question 2 [14 marks] (note – there is a part (a) and (b) for this question)

Part a

(a) Provide Verilog code for the following block design including translating the pseudocode below for the DEV1 and DEV2 blocks into Verilog. Refer to Verilog cheetsheet for syntax. [10 marks].



The pseudocode below describes the implementation of the DEV1 and DEV2 blocks. Note that you need to translate this into Verilog as well (some of it may be close, but it is not real Verilog).

```
void DEV1 ( output bit y, input bit A, input bit B, input bit x) {
  IF (x == A) THEN y = B ELSE y = NOT B;
}
void DEV2 ( output bit x, input bit A, input bit Clk) {
  static bit oldA = 0;
  ON POSITIVE EDGE OF Clk  DO {
       oldA = A;
   }
   x = oldA;
}
```

Part b

(b) How would you go about testing your delta modulation module? (You can give sample code or a sketch if you think this would assist your explanation.) [4 marks]

Question 3 [14 marks]

(a) How do you tell if a computer system is or isn't a reconfigurable computer? [3 marks]
(b) What is the difference between these three things: 1) programmable logic device; 2) programmable logic element (PLE) and 3) programmable logic block (PLB)? [4 marks]
(c) Provide a sketch using multiplexors and flip flips that indicates how interconnects between PLBs within a FPGA are configured. [5 marks]
(d) What is the 'configuration architecture' part of a board designed for using FPGAs? [2 marks]

Question 4 [5 marks]

Over the past decade and a bit, HPEC system design has been swaying from using application specific hardware to general-purpose programmable hardware. Presently the trend is a hybrid approach. Briefly elaborate how this can help to get a good balance for 'SWAP' characteristics. [5 marks]